ER-OLED0.91-1 Series

OLED Display Datasheet

ISO9001
Registered Company
sira
CERTIFICATION
UKAS
QUALITY
MANAGEMENT
011

RoHS
COMPLIANT

EastRising Technology Co., Limited

Attention:

A. Some specifications of IC are not listed in this datasheet. Please refer to the IC datasheet for more details.

B. The related documents for interfacing, demo code, ic datasheet are all available, please download from www.buydisplay.com.

C. Please pay more attention to "Quality Control" in this Datasheet. We assume you already agree with these criterions when you place an order with us. No more recommendations.

REV	DESCRIPTION	RELEASE DATE
1.0	Preliminary Release	May-11-2009

ORDERING INFORMATION

Order Number

Part Number(Order Number)	Description
ER-OLED0.91-1W	0.91"OLED Display Module in White Color
ER-OLED0.91-1B	0.91"OLED Display Module in Blue Color
ER-DBO0.91-1	MCU 8051 Demo Board for ER-OLED0.91-1 Series Products

Image

↑ ER-OLED0.91-1W

↑ ER-OLED0.91-1B
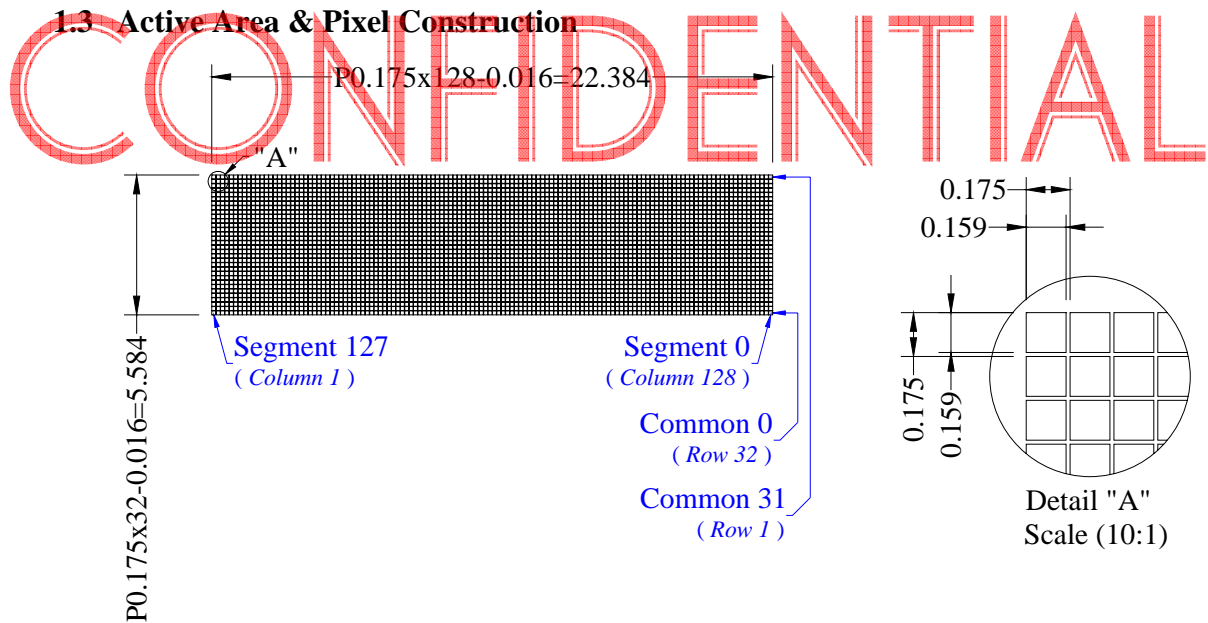
Contents

1. Basic Specifications

1.1 Display Specifications

1) Display Mode: Passive Matrix
2) Drive Duty: 1/32 Duty

1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 128×32
3) Panel Size: $30.0 \times 11.50 \times 1.45$ (mm)
4) Active Area: 22.384×5.584 (mm)
5) Pixel Pitch: 0.175×0.175 (mm)
6) Pixel Size: 0.159×0.159 (mm)
7) Weight: 1.05 (g)

1.3 Active Area & Pixel Construction

P0.175x128-0.016=22.384

"A"

P0.175x32-0.016=5.584

Segment 127
(Column 1)

Segment 0
(Column 128)

Common 0
(Row 32)

Common 31
(Row 1)

0.175
0.159

0.175
0.159

Detail "A"
Scale (10:1)

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1.4 Mechanical Drawing
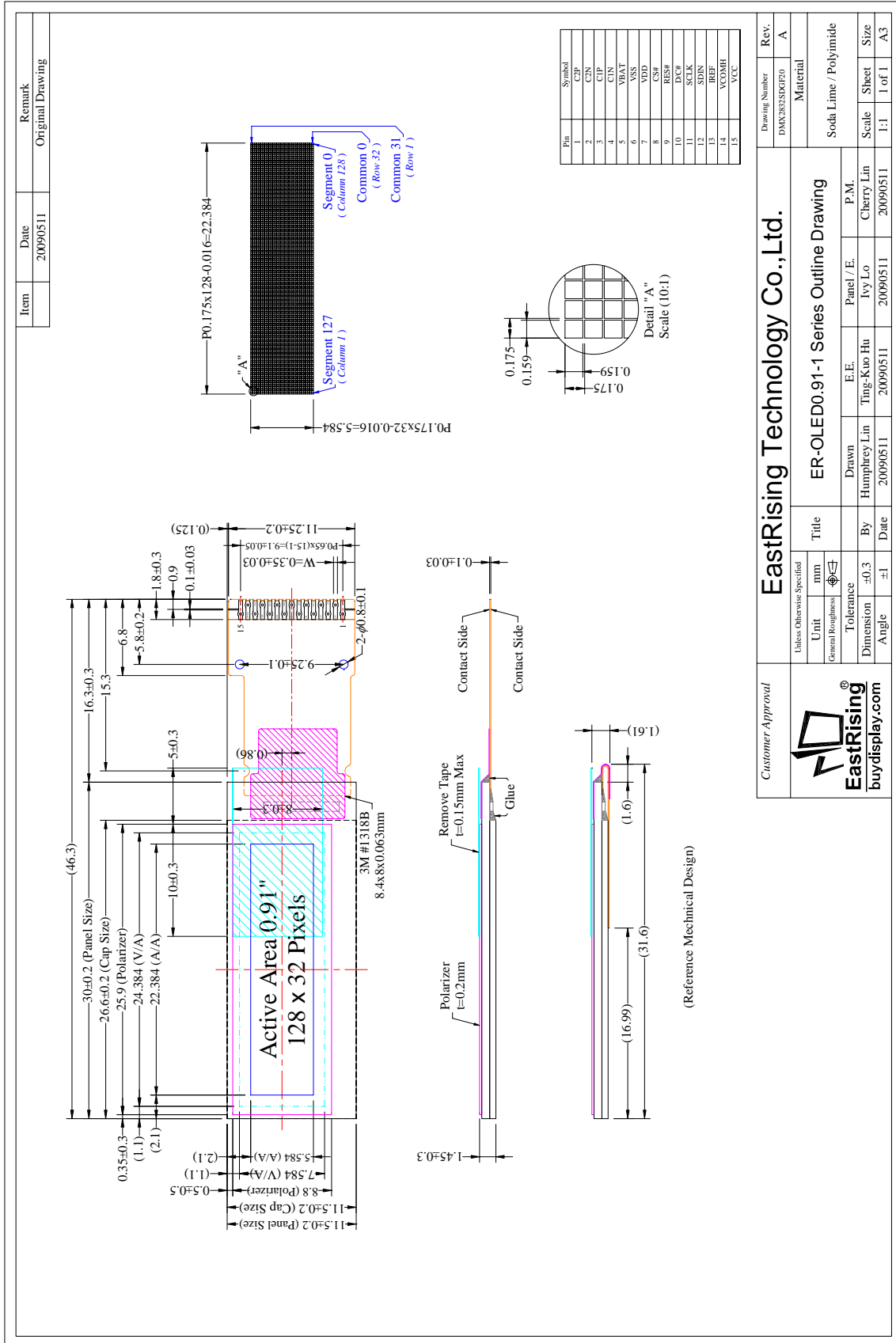
1.5 Pin Definition

Pin Number	Symbol	Type	Function
Power Supply			
7	VDD	P	*Power Supply for Logic* This is a voltage supply pin. It must be connected to external source.
6	VSS	P	*Ground of OEL System* This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.
15	VCC	P	*Power Supply for OEL Panel* This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.
Driver			
13	IREF	I	*Current Reference for Brightness Adjustment* This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 12.5μA.
14	VCOMH	O	*Voltage Output High Level for COM Signal* This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
DC/DC Converter			
5	VBAT	P	*Power Supply for DC/DC Converter Circuit* This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.
3 / 4 1 / 2	C1P / C1N C2P / C2N	I	*Positive Terminal of the Flying Inverting Capacitor* *Negative Terminal of the Flying Boost Capacitor* The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.
Interface			
9	RES#	I	*Power Reset for Controller and Driver* This pin is reset signal input. When the pin is low, initialization of the chip is executed.
8	CS#	I	*Chip Select* This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
10	D/C#	I	*Data/Command Control* This pin is Data/Command control pin. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

1.5 Pin Definition (Continued)

Pin Number	Symbol	Type	Function
Interface (Continued)			
11	SCLK	I	*Serial Clock Input Signal* The transmission if information in the bus is following a clock signal. Each transmission of data bit is taken place during a single clock period of this pin.
12	SDIN	I	*Serial Data Input Signal* This pin acts as a communication channel. The input data through SDIN are latched at the rising edge of SCLK in the sequence of MSB first and converted to 8-bit parallel data and handled at the rising edge of last serial clock. SDIN is identified to display data or command by D/C# bit data at the rising of first SCLK.

1.6 Block Diagram

1.6.1 V_{CC} Supplied Externally

Active Area 0.91"
128 x 32 Pixels

SSD1306
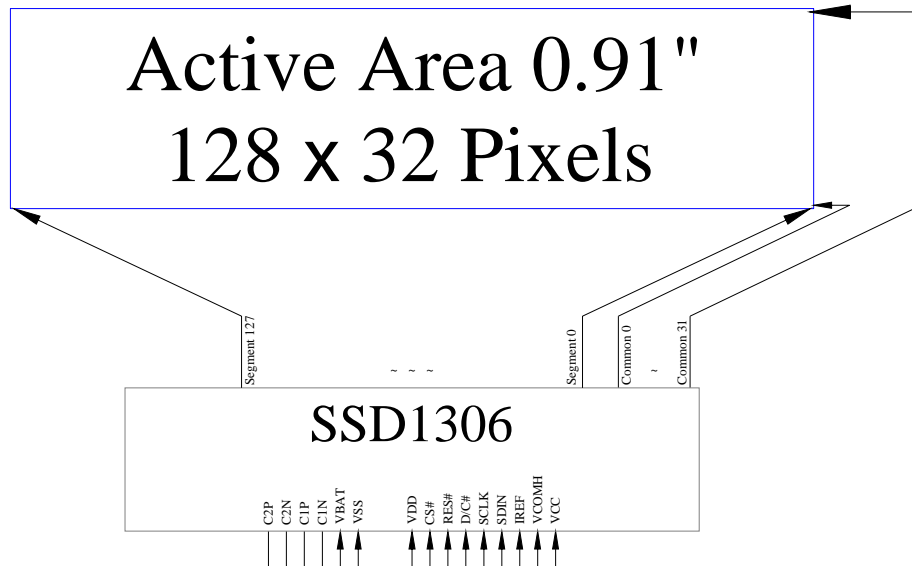
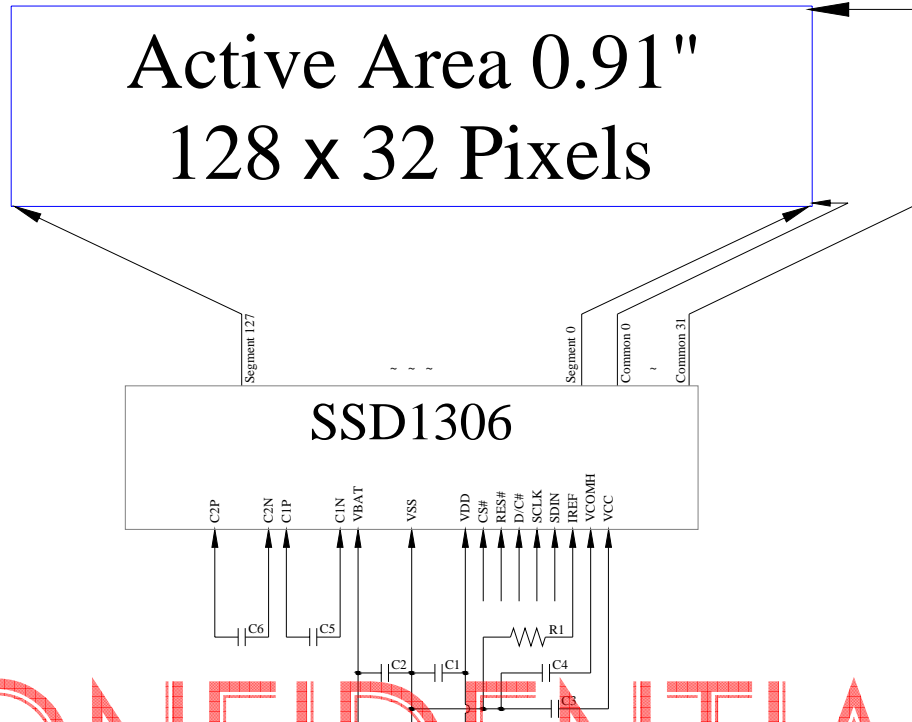Pins connected to MCU interface: CS#, RES#, D/C#, SCLK, and SDIN

C1:   1μF
C2, C3: 2.2μF
R1:   390kΩ, R1 = (Voltage at IREF – VSS) / IREF

1.6.2 V_{CC} Generated by Internal DC/DC Circuit

Pins connected to MCU interface: CS#, RES#, D/C#, SCLK, and SDIN

C1, C2, C5, C6: 1μF
C3, C4:   2.2μF
R1:   390kΩ, R1 = (Voltage at IREF – VSS) / IREF

2. *Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	11	V	1, 2
Operating Temperature	T_{OP}	-30	70	°C	-
Storage Temperature	T_{STG}	-40	80	°C	-

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

3. *Optics & Electrical Characteristics*

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer (Note 3)	120	150	-	cd/m^2
C.I.E. (White)	(x) (y)	Without Polarizer	0.26 0.29	0.32 0.33	0.34 0.37	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 7.25V.
  Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}	-	1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	V_{CC}	Note 3	7	7.25	7.5	V
Supply Voltage for DC/DC	V_{BAT}	*Internal DC/DC Enable*	*3.3*	*-*	*4.2*	*V*
Supply Voltage for Display (Generated by Internal DC/DC)	V_{CC}	*Note 3*	*7*	*7.25*	*7.5*	*V*
High Level Input	V_{IH}	-	0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}	-	0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.1×V_{DD}	V
Operating Current for V_{DD}	I_{DD}	-	-	180	300	μA
Operating Current for V_{CC} (V_{CC} Supplied Externally)	I_{CC}	Note 4	-	4.3	5.4	mA
		Note 5	-	6.8	8.5	mA
Operating Current for V_{BAT} (V_{CC} Generated by Internal DC/DC)	I_{BAT}	*Note 4*	*-*	*12.6*	*15.8*	*mA*
		Note 5	*-*	*18.4*	*23.0*	*mA*
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$	-	-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$	-	-	1	5	μA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 4: V_{DD} = 2.8V, V_{CC} = 7.25V, 50% Display Area Turn on.
Note 5: V_{DD} = 2.8V, V_{CC} = 7.25V, 100% Display Area Turn on.

* Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)
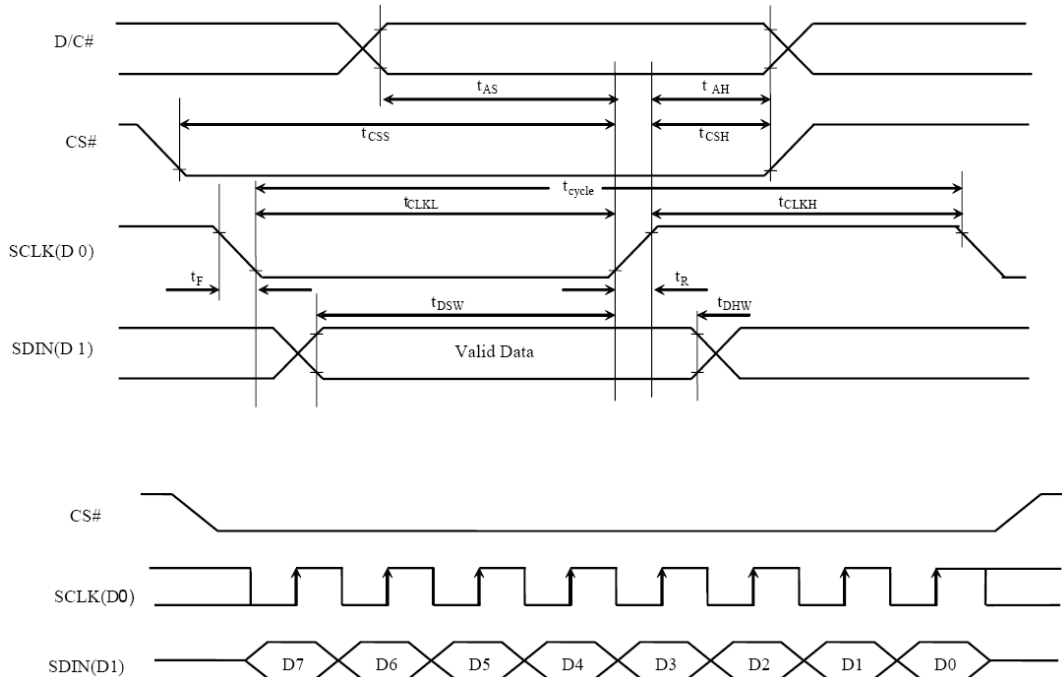
4. Functional Specification

4.1. Commands

Refer to the Technical Manual for the SSD1306

#### 4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command

4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
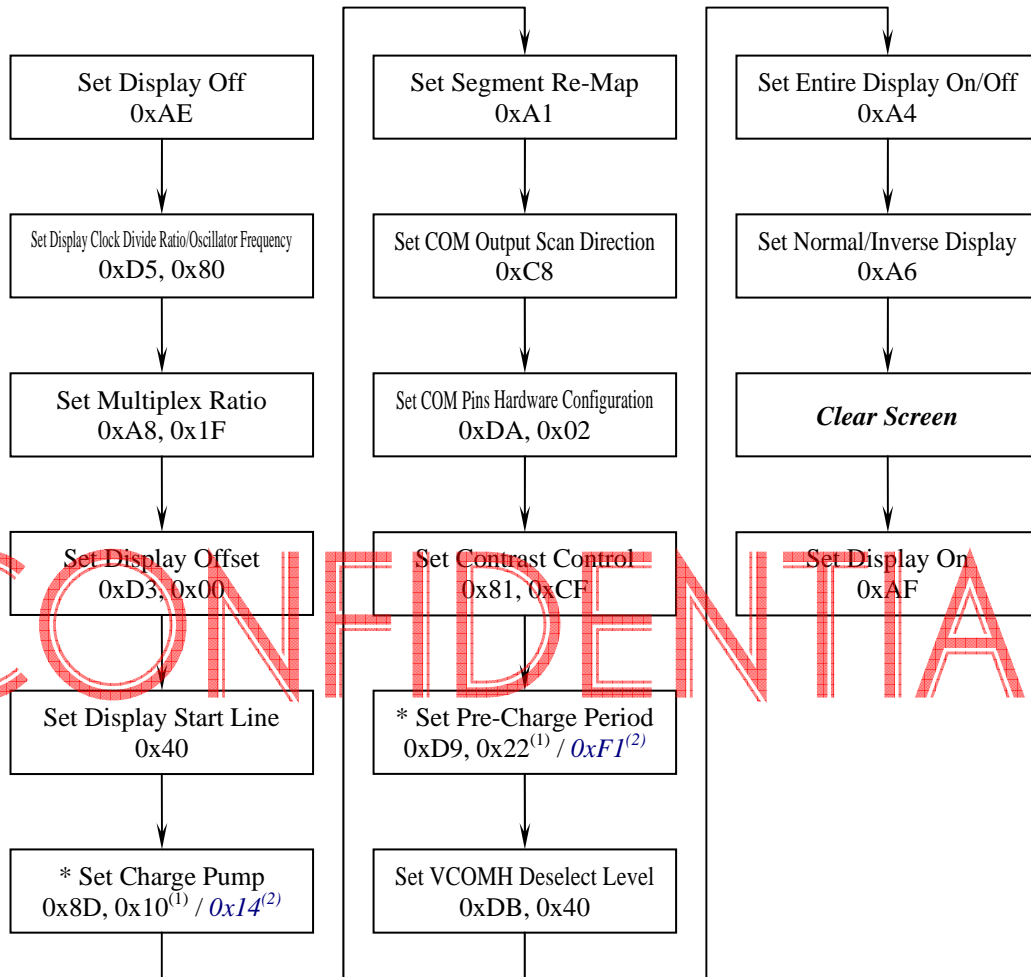4. Power down V_{DD}
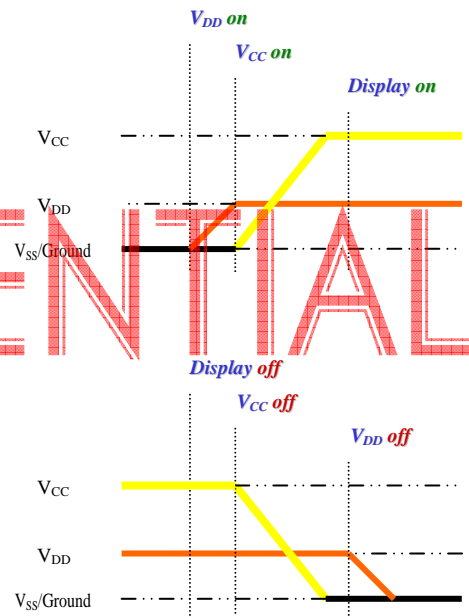
4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:
1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization>

Set Display Off 0xAE	Set Segment Re-Map 0xA1	Set Entire Display On/Off 0xA4
Set Display Clock Divide Ratio/Oscillator Frequency 0xD5, 0x80	Set COM Output Scan Direction 0xC8	Set Normal/Inverse Display 0xA6
Set Multiplex Ratio 0xA8, 0x1F	Set COM Pins Hardware Configuration 0xDA, 0x02	*Clear Screen*
Set Display Offset 0xD3, 0x00	Set Contrast Control 0x81, 0xCF	Set Display On 0xAF
Set Display Start Line 0x40	* Set Pre-Charge Period 0xD9, 0x22$^{(1)}$ / *0xF1$^{(2)}$*	
* Set Charge Pump 0x8D, 0x10$^{(1)}$ / *0x14$^{(2)}$*	Set VCOMH Deselect Level 0xDB, 0x40	

* Written Value for Parameters
    [1] ➔ V$_{CC}$ Supplied Externally
    [2] ➔ *V$_{CC}$ Generated by Internal DC/DC Circuit*

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	
Low Temperature Operation	-30°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	The operational functions work.
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness reached.

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	10,000	-	hr	120 cd/m^2, 50% Checkerboard	6
Storage Life Time	20,000	-	hr	T_a = 25°C, 50% RH	-

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. QUALITY CONTROL

6.1 EastRising Environment Required

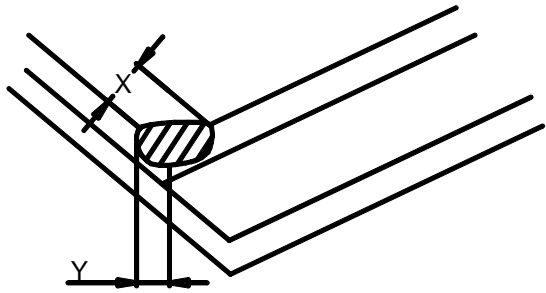Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23±5℃
Humidity:	55±15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥50cm
Distance between the Panel & Eyes of the Inspector:	≥30cm

Finger glove (or finger cover) must be worn by the inspector.
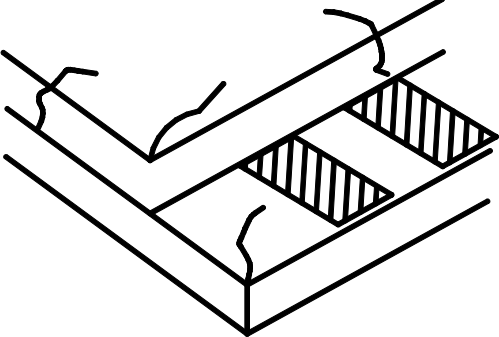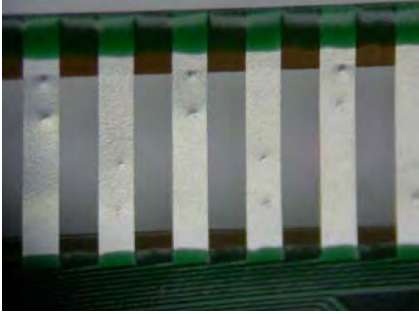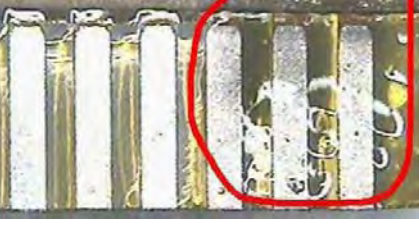
Inspection table of jig must be anti-electrostatic.

6.2 EastRising OLED Display Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

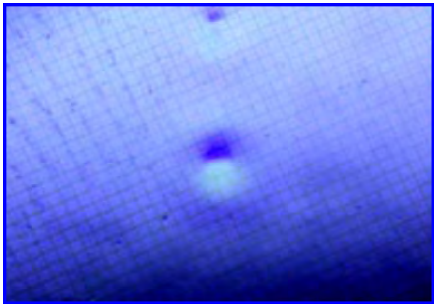6.2.1 EastRising Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X>6mm (Along with Edge) Y>1mm (Perpendicular to edge)

6.2.2 EastRising Cosmetic Check (Display Off)in Non-Active Area (Continued)

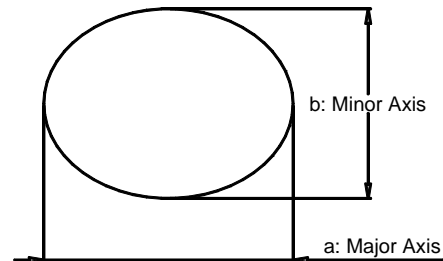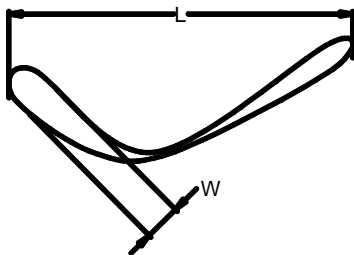| Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Termial Lead Prober Mark	Acceptable	
Glue or Contamination on Pin	Minor	
Ink marking on Back Side of Panel (Exclude on Film)	Acceptable	Ignore for Any

6.2.3 EastRising Cosmetic Check (Display Off) in Active Area

EastRising recommends to execute in clear environment (class 10k) if actual in necessary.
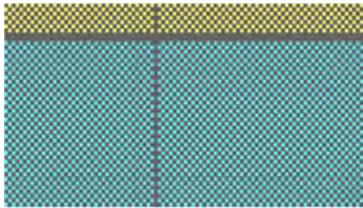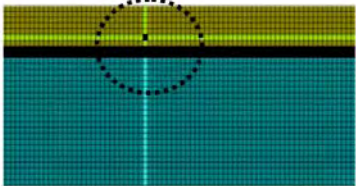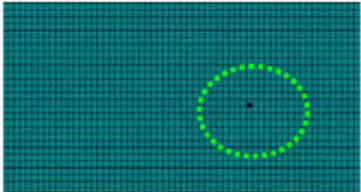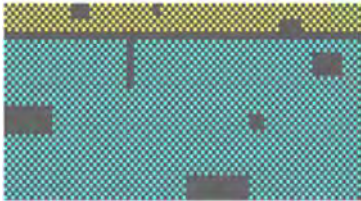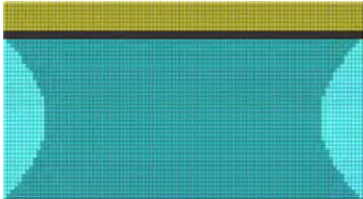
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches,Fiber,Line-Shape Defect (On Polarizer)	Minor	W≤0.1 Ignore W＞0.1 L≤2 n≤1 L＞2 n＝0
Dirt, Black Spot, Foreign Material (On Polarizer)	Minor	Φ≤0.1 Ignore 0.1＜Φ≤0.25 n≤1 0.25＜Φ n＝0
Dent,Bubbles,White Spot (Any Transparent Spot on Polarizer)	Minor	Φ≤0.5 Ignore if no Influence on Display 0.5＜Φ n＝0
Fingerpint ,Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

* Definition of W & L &Φ(Unit:mm): Φ=(a+b)/2

6.2.4 EastRising Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7.PRECAUTIONS for USING

7.1 Handling Precautions

1) Since the EastRiisng OLED display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.

2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.

3) If pressure is applied to the display surface or its neighborhood of the EastRising OLED display module, the cell structure may be damaged and be careful not to apply pressure to these sections.

4) The polarizer covering the surface of the OLED display module is soft and easily scratched.   Please be careful when handling the OLED display module.

5) When the surface of the polarizer of the OLED display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
    * Scotch Mending Tape No. 810 or an equivalent
    Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy. Also, pay attention that the following liquid and solvent may spoil the polarizer:
    * Water
    * Ketone
    * Aromatic Solvents

6) Hold EastRising OLED display module very carefully when placing OLED display module into the system housing. Do not apply excessive stress or pressure to OLED display module.   And, do not over bend the film with electrode pattern layouts.   These stresses will influence the display performance.   Also, secure sufficient rigidity for the outer cases.

7) Do not apply stress to the driver IC and the surrounding molded sections.

8) Do not disassemble nor modify the OLED display module.

9) Do not apply input signals while the logic power is off.

10) Pay sufficient attention to the working environments when handing EastRising OLED display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OLED display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.

* Protective film is being applied to the surface of the display panel of the OLED display module.
Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the EastRising OLED display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

12) If electric current is applied when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

7.2 Storage Precautions

1) When storing EastRising OLED display modules, put them in static electricity preventive bags avoiding exposure neither to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high
humidity environment or low temperature (less than 0℃) environments. (We recommend you to store these modules in the packaged state when they were shipped from EastRising.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

2) If electric current is applied when water drops are adhering to the surface of the OLED display module, when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

7.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OLED display module, and if these values are exceeded, panel damage may be happen.

2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.

3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)

4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.

5) As for EMI, take necessary measures on the equipment side basically.

6) When fastening the OLED display module, fasten the external plastic housing section.

7) If power supply to the EastRising OLED display module is forcibly shut down by such errors as taking out the main battery while the OLED display panel is in operation, we cannot guarantee the quality of this OLED display module.

7.4 Precautions when disposing of the EastRising OLED display modules
1) Request the qualified companies to handle industrial wastes when disposing of the OLED display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

7.5 Other Precautions
1) When an OLED display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored.   Also, there will be no problem in the reliability of the module.

2) To protect OLED display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OLED display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC

3) With this OLED display module, the OLED driver is being exposed.   Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OLED driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OLED driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OLED driver may be shielded from light during the inspection processes.

4) Although this OLED display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

That's the end of the datasheet.